Amendments to the Specification

IN THE ABSTRACT OF THE DISCLOSURE

Attached hereto is a replacement (or new) Abstract.

IN THE WRITTEN DESCRIPTION

Please delete the paragraph beginning at page 12, line 2.

Please replace the paragraph beginning at page 12, line 6, with the following rewritten paragraph:

C1

Preferred embodiments of the invention are described below with reference to the drawings. In these embodiments, the efficiency of trilinear texture filtering is improved by the generation of the lower-level texture mip-map on the fly from the upper-level mip-map, and with the use of texture caching and texture decompression as a means of meeting the high memory bandwidth requirements. Removing the need to read the lower-level mip-map in a separate memory access, removes page break problems and enhances performance.

Please replace the paragraph beginning at page 13, line 29, with the following rewritten paragraph:

C2

~~Figure 6 illustrates~~Figures 6A and 6B illustrate the storage of texture words in a worst-case scenario;

Please replace the paragraph beginning at page 14, line 1, with the following rewritten paragraph:

C3

~~Figure 8 illustrates~~Figures 8A and 8B illustrate in similar manner to ~~Figure 6~~Figures 6A and 6B the storage of texture words in a best-case scenario;

Please replace the paragraph beginning at page 15, line 32, with the following rewritten paragraph:

C4

The lower-level mip-map is generated by four parallel filters or interpolators 40 that are able to take the 16 upper-level texels and generate the four lower level in one clock cycle. Figure 5 illustrates this process. Out of the 16

original texels, four are decoded to produce the four upper-level texels which are directly used for trilinear filtering. These 16 are also divided into four quadrants, each containing four ~~pixels~~texels, which are then filtered by four digital low-pass filters to produce the four lower-level mip-map texels required for trilinear filtering. This filtering algorithm is shown in Equation 3:

Please replace the paragraph beginning at page 17, line 28, with the following rewritten paragraph:

The embodiment of the invention illustrated in Figure 4 shows how one cache 30 and one decompression unit (DU) 32 are required to return all data necessary to construct a complete trilinear interpolated pixel. A problem exists, however, when the filter algorithm needs data from two or four additional data words. Figure 6 shows the worse case situation. Consider the texture bitmap divided into tiles, with each tile representing the texture pixels provided by one compressed data word. In this example the data word contains 16 texture pixels. The darker outlined boxes in ~~Figure 6~~Figures 6A and 6B represent the tiles. In this example, the filter algorithm requires texture pixels from four separate compressed data words. For a single cache/decompression system, this worst case situation requires four cache reads and therefore a minimum of four clock cycles. This problem also exists, to a lesser extent, when two separate data words are required.

Please replace the paragraph beginning at page 19, line 30, with the following rewritten paragraph:

The caches 60 for the quad cache system are effectively memory mapped, i.e. each cache holds data for a separate tile of texture memory, as noted above. However, the DUs 62 do not necessarily have to be memory mapped as well. Memory mapping of DUs would require that each is associated with a particular cache. This would also necessitate each DU being able to produce at least four upper-level texels as well as four

C6 lower-level texels in one cycle to cater for the best case situation. The best case situation is illustrated in ~~Figure 8~~Figures 8A and 8B where all the tiles come from one data word.

Please add the following new paragraph after the paragraph ending on line 4 of page 24:

C8 What is claimed is: